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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **RCA89647**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 10/030796

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US99/30775	**22 December 1999 (22.12.99)**	**15 July 1999 (15.07.99)**

TITLE OF INVENTION

METHOD AND APPARATUS FOR ISOLATING IIC BUS NOISE FROM A TUNER IN A TELEVISION RECEIVER

APPLICANT(S) FOR DO/EO/US

David Glen White and Matthew Thomas Mayer

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☒ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

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EXPRESS MAIL LABEL NO. EL902321767US **DATE DEPOSITED: January 11, 2002**

U.S. APPLICATION NO: (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/030796	PCT/US99/30775	RCA89647

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1040.00
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	$890.00
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$740.00
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$710.00
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	$0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	11 - 20 =	0	x $18.00	$0.00	
Independent claims	3 - 3 =	0	x $84.00	$0.00	
Multiple Dependent Claims **(check if applicable).**			☐	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				$0.00	
SUBTOTAL =				$890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				$0.00	
TOTAL NATIONAL FEE =				$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				$40.00	
TOTAL FEES ENCLOSED =				$930.00	
				Amount to be: refunded	$
				charged	$ 930.00

a. ☐ A check in the amount of _____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. **07-0832** in the amount of **$930.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **07-0832** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Mr. Joseph S. Tripoli
THOMSON multimedia Licensing Inc.
Patent Department
PO Box 5312
Princeton, New Jersey 08540

SIGNATURE

PAUL P. KIEL
NAME

40,677
REGISTRATION NUMBER

January 11, 2002
DATE

EXPRESS MAIL LABEL NO. EL902321767US RCA 89647

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : David Glen White and Matthew Thomas Mayer

Filed : Herewith

For : METHOD AND APPARATUS FOR ISOLATING IIC BUS NOISE FROM A TUNER IN A TELEVISION RECEIVER

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/US99/30775 filed herewith, please enter the following amendments:

IN THE SPECIFICATION:

Please amend the specification as follows:

On Page 1, line 3, please insert the following paragraph:

--This application claims the benefit under 35 U.S.C. § 365 of International Application PCT/US99/30775, filed December 22, 1999, which was published in accordance with PCT Article 21(2) on January 25, 2001 in English; and which claims benefit of U.S. provisional application serial no. 60/143,845 filed July 15, 1999.--

IN THE CLAIMS:

Please amend the claims (which are the annexes of the International Preliminary Examination Report) as follows. A marked-up version of the claims is attached herewith.

1.(AMENDED) An apparatus for isolating a noise intolerant device from a source of noise, comprising:

a processor for producing clock and data signals and a control signal; and

a digital bus that couples said clock and data signals to a buffer,

where, in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device.

2.(AMENDED) The apparatus of claim 1, wherein said digital bus is an inter integrated circuit bus, and the apparatus further comprises an IIC bus expander for transferring said control signal to said buffer.

3. (AMENDED) The apparatus of claim 1, wherein the digital bus comprises

an IIC bus having a clock signal path for transferring clock pulses from said processor to said clock inputs of said IIC bus expander and said buffer;

a data signal path for transferring data from said processor on said data signal path during each of said clock pulses on said clock signal path to said clock and data inputs of said IIC bus expander and said buffer; and

wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device from said IIC bus and said processor.

4. (AMENDED) The apparatus of claim 3, wherein said noise intolerant device comprises:

a tuner, coupled to said clock and data outputs of said buffer device, having a phase-lock loop for generating frequency variable tones, and a down-converter coupled, to said phase-lock loop, for mixing one of a plurality of television signals with a one of said frequency variable tones to produce an IF television signal.

5. (AMENDED) The apparatus of claim 4, wherein said buffer comprises:

a first OR gate and a second OR gate, each of said first and said second OR gates having a first input coupled to said output of said IIC bus expander;

a second input said first OR gate coupled to a clock signal path of said IIC bus, and a second input of said second OR gate coupled to a data signal path of said IIC bus; and

an output of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop, and an output of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop.

6.(AMENDED) A television receiver for receiving and processing television signals, apparatus comprising:

a controller assembly comprising an inter-integrated circuit bus having a clock signal path and a data signal path, a processor, coupled to said clock and data paths, an IIC bus expander coupled to said processor via said clock and data paths, and a buffer coupled to an output of said IIC bus expander;

a front-end assembly comprising a tuner having a down converter coupled to a phase-lock loop, said phase-lock loop coupled to an output of said buffer, at least one demodulator for demodulating said television signals, coupled to said down-converter, such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device; and

at least one video and audio processor for processing said modulated television signals to produce audio and video signals.

7.(AMENDED) The apparatus of claim 6, wherein said buffer comprises:

a first OR gate and a second OR gate, each of said first and said second OR gates having a first input coupled to said output of said IIC bus expander;

a second input of said first OR gate coupled to said clock signal path of said IIC bus, and a second input of said second OR gate coupled to said data signal path of said IIC bus; and

an output of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop, and an output of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop.

8. (AMENDED) A method for isolating a phase-lock loop in a tuner of a television receiver, comprising the steps of:

sending a first command from a processor to a phase-lock loop via a digital bus to generate a frequency tone; and

sending a second command to a buffer to isolate said phase-lock loop from said processor, whereby said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device

9. (AMENDED) The method of claim 8, wherein said first command sending step further comprises the steps of:

setting an inter-integrated circuit bus expander output to a LOW logical state, after receiving a request for a selected television signal from a user, in response to said first command by said processor; and

coupling said phase-lock loop to an IIC bus, for enabling said processor to communicate with said phase-lock loop to generate said frequency tone.

10. The method of claim 9 wherein said coupling step further comprises the step of:

enabling, in response bus expander output, a buffer to couple said phase-lock loop to said IIC bus.

11. The method of claim 9, wherein said second command sending step further comprises the step of:

setting an output of said buffer to a HIGH logical state after said phase-lock loop locks to said single frequency tone, in response to said second command from said processor.

IN THE ABSTRACT:

Please add the following Abstract.

-- A method and apparatus for isolating a noise intolerant device, e.g., a phase-lock loop of a tuner within a television receiver, from source of noise. In one embodiment, the apparatus isolates a phase-lock loop integrated circuit from the bus, by providing an isolation buffer that allows the receiver to only pass data to the tuner's phase-lock loop IC when a tune command is issued by a processor. When not being tuned, the IIC lines to the tuner are held HIGH by a buffer until needed again to perform the tuning function. This allows the demodulation circuitry to use a setting for a carrier tracking-loop that optimizes bit error rate performance.--

REMARKS

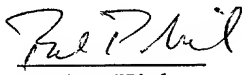
The specification has been amended to include a reference to the priority applications.

Claims 1-9 are amended to remove reference indicia.

To meet the requirements of the United States, the Abstract (as originally filed in the PCT application) is added.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
David Glen White
Matthew Thomas Mayer



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January 11, 2002

MARKED UP VERSION OF THE AMENDED CLAIMS

1.(AMENDED) An apparatus for isolating a noise intolerant device [(140)] from a source of noise, comprising:

a processor [(106)] for producing clock and data signals [(SCL, SDA)] and a control signal; and

a digital bus [(118)] that couples said clock and data signals to a buffer [(114)],

where, in response to said control signal [(109)], said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device.

2.(AMENDED) The apparatus of claim 1, wherein said digital bus is an inter integrated circuit [(IIC)] bus, and the apparatus further comprises an IIC bus expander [(108)] for transferring said control signal to said buffer.

3. (AMENDED) The apparatus of claim 1, wherein the digital bus comprises

an IIC bus having a clock signal path [(SCL)] for transferring clock pulses from said processor [(106)] to said clock inputs of said IIC bus expander [(108)] and said buffer [(114)];

a data signal path [(SDA)] for transferring data from said processor [(106)] on said data signal path during each of said clock pulses on said clock signal path to said clock and data inputs of said IIC bus expander [(108)] and said buffer [(114)]; and

wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device [(140)] from said IIC bus and said processor.

4. (AMENDED) The apparatus of claim 3, wherein said noise intolerant device comprises:

a tuner [(140)], coupled to said clock and data outputs of said buffer device, having a phase-lock [(142)] loop for generating frequency variable tones, and a down-converter [(144)] coupled, to said phase-lock loop, for mixing one of a plurality

of television signals with a one of said frequency variable tones to produce an IF television signal.

5. (AMENDED) The apparatus of claim 4, wherein said buffer [(144)] comprises:

a first OR gate [(116)] and a second OR gate [(117)], each of said first and said second OR gates having a first input [(116_1, 117_1)] coupled to said output of said IIC bus expander;

a second input [(116_2)] said first OR gate coupled to a clock signal path of said IIC bus, and a second input [(117_2)] of said second OR gate coupled to a data signal path of said IIC bus; and

an output [(116_3)] of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop [(142)] , and an output [(117_3)] of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop [(142)].

6.(AMENDED) A television receiver [(100)] for receiving and processing television signals, apparatus comprising:

a controller assembly [(102)] comprising an inter-integrated circuit [(IIC)] bus having a clock signal path [(110)] and a data signal path [(112)], a processor [(106)], coupled to said clock and data paths, an IIC bus expander [(109)] coupled to said processor via said clock and data paths, and a buffer [(114)] coupled to an output of said IIC bus expander;

a front-end assembly [(130)] comprising a tuner [(140)] having a down converter [(144)] coupled to a phase-lock loop [(142)], said phase-lock loop coupled to an output of said buffer [(114)], at least one demodulator [(131, 132)] for demodulating said television signals, coupled to said down-converter, such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device; and

at least one video and audio processor [(122, 124)] for processing said modulated television signals to produce audio and video signals.

7.(AMENDED) The apparatus of claim 6, wherein said buffer comprises:

a first OR gate [(116)] and a second OR gate [(117)], each of said first and said second OR gates having a first input [(116_1, 117_1)] coupled to said output of said IIC bus expander;

a second input [(116_2)] of said first OR gate coupled to said clock signal path of said IIC bus, and a second input [(117_2)] of said second OR gate coupled to said data signal path of said IIC bus; and

an output [(116_3)] of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop [(143)], and an output [(117_3)] of said second OR gate, being said data output of said buffer [(114)], coupled to said data input of said phase-lock loop.

8. (AMENDED) A method for isolating a phase-lock loop in a tuner of a television receiver, comprising the steps of:

sending [(208)] a first command from a processor to a phase-lock loop via a digital bus to generate a frequency tone; and

sending [(210)] a second command to a buffer to isolate said phase-lock loop from said processor, whereby said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device

9. (AMENDED) The method of claim 8, wherein said first command sending step further comprises the steps of:

setting an inter-integrated circuit [(IIC)] bus expander output to a LOW logical state, after receiving a request for a selected television signal from a user, in response to said first command by said processor; and

coupling said phase-lock loop to an IIC bus, for enabling said processor to communicate with said phase-lock loop to generate said frequency tone.

10. The method of claim 9 wherein said coupling step further comprises the step of:

enabling, in response bus expander output, a buffer to couple said phase-lock loop to said IIC bus.

11. The method of claim 9, wherein said second command sending step further comprises the step of:

setting an output of said buffer to a HIGH logical state after said phase-lock loop locks to said single frequency tone, in response to said second command from said processor.

METHOD AND APPARATUS FOR ISOLATING IIC BUS NOISE FROM A TUNER IN A TELEVISION RECEIVER

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a television receiver. More particularly, the invention relates to a method of reducing phase noise interference in a phase lock loop circuit of a television receiver.

Description of the Background Art

A typical high definition television (HDTV) system employs a front end comprising a tuner, a digital IF circuit and a digital demodulation integrated circuit (IC). The system is controlled from the digital decoder board using an inter-integrated circuit bus (I^2C). The terminology IIC bus, I2C bus or I^2C bus are equivalent, as used herein.

The IIC bus is a two wire, bi-directional bus that permits only two integrated circuits (IC's) to communicate on a bus path at a time. An IC serving in a "master" mode of operation, initiates a data transfer on the bus and generates clock signals that permit the data transfer. An IC serving in a "slave" mode of operation is the IC being operated on or communicated to by the master IC, whereby the slave IC is instructed to either send or receive data. Each IC has its own unique seven bit address, wherein the master IC initiates the communications, and also terminates the communications.

A serial clock line (SCL) propagates clock signals on the IIC bus from a master IC to a slave IC. Each master IC generates its own clock signals when transferring data on the bus. The second bi-directional wire of the IIC bus is a serial data line (SDA) that transfers data using eight bit serial transactions. Typically, a ninth bit is utilized as an acknowledgment bit. When both clock and data lines are held "HIGH", no data can be transferred between two IC's. A HIGH to LOW transition on the SDA line, while the SCL line is HIGH, indicates a start condition for the exchange of data bits. Conversely, a LOW to HIGH

transition on the SDA line, while the SCL line is HIGH, defines a stop condition. The master IC generates one clock pulse for each data bit transferred on the SDA line, and the HIGH or LOW state of the data line can only change when the clock signal on the SCL line is in a LOW state.

Multiple IC's share the IIC bus. For example, a microprocessor, in a controller of a television receiver, communicates with numerous IC's within the television receiver via an IIC bus. A problem has been uncovered when down-converting a television signal to a specific intermediate frequency (IF) signal. Coincidental bus traffic by the microprocessor, which functions as a master IC, has been found to cause phase noise interference in a tuner of the receiver. Specifically, a phase-lock loop (PLL) integrated circuit is serially coupled on the IIC bus in the tuner of the television receiver, and acts as a frequency variable tone generator. The microprocessor controls the oscillator frequency of the PLL via the IIC bus. The phase-lock loop is susceptible to the bus traffic when the microprocessor sends commands to other IC's on the bus, so that instead of producing a tone locked at a specific frequency, a range of other frequencies around the desired tone frequency are produced.

For example, in a PLL having a 4 Mhz oscillator, any incidental noise signals generated by the microprocessor may be received by other pins of the PLL integrated circuit connected to the IIC bus. This noise will be added to the resultant signal frequency. In an instance where a user selects a channel at 701 Mhz and the receiver system requires a down-converted IF signal at 44 Mhz, then the PLL must generate a tone locked at a frequency of 745 Mhz. Normally, the 701 Mhz television signal and the 745 Mhz tone signal are mixed to produce an IF signal locked at 44 Mhz. However, additional noise will generate other harmonic frequencies around the tone frequency, causing the IF frequency to fluctuate in a range around 44 Mhz instead.

Thus, the bus chatter is added to the incoming digital video/audio signal and causes a degradation in bit error rate (BER) performance of the television receiver. Ultimately, the bit errors manifest themselves as additional or missing luminance and chrominance pixel components in the video the user is viewing, as well as "clicks and pops" in the audio output. Similarly, when processing an

analog television signal, the IIC bus chatter will manifest itself as a distorted picture and/or undesirable wow and/or flutter in the audio output.

Phase noise interference, caused by the IIC bus traffic, may be compensated somewhat by widening the bandwidth of the demodulation IC's carrier tracking-loop, to allow it to "track out" the corruption. However, such a method allows additional low frequency noise to combine with the video/audio signal, thereby degrading the bit error rate of the television receiver.

Thus, there is a need to reduce the IIC bus chatter created by the IC traffic on the IIC bus. Furthermore, there is a need to reduce the IIC bus chatter before it influences the phase-lock loop circuitry of the tuner.

SUMMARY OF INVENTION

The disadvantages heretofore associated with the prior art, are overcome by the present invention of a method and apparatus for isolating a noise intolerant device, e.g., a phase-lock loop of a tuner within a television receiver, from source of noise. In one embodiment, the apparatus isolates a phase-lock loop integrated circuit (IC) from the bus, by providing an isolation buffer that allows the receiver to only pass data to the tuner's phase-lock loop IC when a tune command is issued by a processor.

When not being tuned, the IIC lines to the tuner are held HIGH by a buffer until needed again to perform the tuning function. This allows the demodulation circuitry to use a setting for a carrier tracking-loop that optimizes bit error rate performance.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIGS. 1A and 1B depict a block diagram of a portion of a television receiver comprising a buffer for an IIC bus; and

FIG. 2 depicts a flow diagram of a method for isolating the tuner from the controller assembly in accordance with the present invention.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION OF THE INVENTION

The invention will be primarily described within the context of a television receiver that receives audio and video television signals. However, it will be appreciated by those skilled in the art that the invention is well suited to any system in which digital signals are communicated on an I2C bus. Other signals and systems may illustratively include, but are not limited to, isochronous information transmitted to a television receiver, or digitized data that is transmitted between computers through cable modems on a cable system. FIGS. 1A and 1B together depict a block diagram of a portion of a television receiver (referred to hereinafter as receiver 100) comprising a buffer 114 for an IIC bus 118 in accordance with the present invention.

The receiver 100 comprises a controller assembly 102 (FIG. 1A), for selecting television signals 120 using an input device 104. The controller assembly 102 comprises a processor 106, a bus expander 108, and a buffer 114. A tuner 140 (FIG. 1B) comprises at least one phase-lock loop 142 and at least one down-converter 146, for tuning and down-converting the television signal 120. The tuner 140 is coupled from an output of the buffer 114 to an input of the phase-lock loop 142. The buffer 114 selectively controls data transmission to the tuner 140. The terminology processor and microprocessor are considered interchangeable, for purposes herein.

In this manner, the traffic noise from the microprocessor 106, which is generated when the microprocessor 106 is communicating with other receiver IC's 105 in the system, will be excluded from passing to the phase-lock loop 142. The elimination of noise from the phase-lock loop 142 permits the phase-lock loop 142 to lock at a specific frequency, and then generate a clear tone for mixing with the frequency down-converter 144. Thus, a substantially noise free IF television signal is produced.

Specifically, the receiver 100 comprises a front-end assembly 130 (FIG. 1B) having at least one tuner 140, at least one digital demodulator 131 and at

least one analog demodulator 132, a digital IF down-converter 133 and an analog IF down-converter 134 to selectively tune, demodulate or otherwise "receive" at least one of a plurality of television signals 120, having audio and video information transmitted in either analog or digital formats. The analog formats include conventional analog broadcasting systems such as those conforming to the NTSC transmission standards. The digital formats include Digital Broadcast Satellite (DBS), Digital Video Broadcasting (DVB), as well as terrestrial broadcast such as high definition television (HDTV) and cable formats, each conforming, for example, to the ATSC and MPEG transmission standards.

A controller assembly102 (FIG. 1A) is coupled to the front-end assembly 130 (FIG. 1B) through an input clock line 145 and an input data line 146 of the phase-lock loop 142. The controller assembly 102 allows a user to select and tune the front-end assembly 130 to any one of the television signals 120. The user makes a channel selection through an input device 104, such as a remote control, and the controller assembly 102 sends a channel selection signal through the IIC bus 118 to the front-end assembly 130.

The front-end assembly 130, in response to the channel selection signal provided by the controller 102, operates to tune a selected television signal 120 for reception. In the instance where the selected television signal is a digital television signal, such as a HDTV channel, the digital demodulator 131 of the front-end assembly 130 demodulates the bit stream. The demodulated digital IF signal is then sent for processing at the MPEG transport processor 126. The MPEG transport processor 126 separates the video and audio signal information and sends such video and audio information to a video processor 122 (via signal path 123) and an audio processor 124 (via signal path 125), respectively.

In the instance where an analog television signal is selected, an analog demodulator 132 of the front end assembly 130 demodulates the video and audio information within the selected television signal, and provides the video and audio information to the video processor 122 and the audio processor 124, respectively. Thus, in an analog signal circumstance, it is not necessary to send the demodulated audio/video IF signal to the MPEG transport processor 126. Finally, after either the digital or the analog baseband signal has been recovered,

the video processor 122 and the audio processor 124 process the video and audio information, and then send the video and audio information to their output devices, such as a display panel and speaker.

In particular, the controller assembly 102 comprises a microprocessor 106 coupled to a bus expander 108, via the IIC bus 118 serial clock and data signal paths 110 and 112, and a plurality of other receiver IC's 105 also coupled to the IIC bus for other data processing purposes. The microprocessor 106 functions as a master IC on the IIC bus, and controls the IIC bus 118 at all times. As such, all of the remaining IC's coupled to the IIC bus 118 operate in a slave mode of operation.

The bus expander IC 106 is coupled to the IIC bus 118 to enable non-IIC compliant IC's to interface with the IIC compliant IC's on the IIC bus 118. The bus expander IC 106 is further coupled to a buffer 114. The buffer 114 comprises a pair of OR gates 116 and 117. However, a person skilled in the art for which the invention pertains will recognize that other buffering devices, such as discrete transistor circuits, may also be utilized.

An output control port 109 of the bus expander 108 is coupled to both the first and second OR gates 116 and 117, through first input ports 116_1 and 117_1 on each OR gate 116 and 117. Additionally, a serial clock line 110 is coupled to a second input port 116_2 on the first OR gate 116. Similarly, a serial data line 112 is coupled to a second input port 117_2 on the second OR gate 117. The pair of OR gates 116 and 117 are then coupled to a tuner 140 in the front-end receiver 130, through their respective output ports 116_3 and 117_3. The output port of the first OR gate 116_3 is coupled to the input clock line 145 of the phase-lock loop 142. Furthermore, the output port of the second OR gate 117_3 is coupled to the input data line 146 of the phase-lock loop 142.

In operation, the microprocessor 106 sends a command signal to the bus expander 108 to set the bus expander's output control port 109 to a logically HIGH state. The bus expander's 108 internal circuitry (not shown) sets the control port 109 HIGH, thereby setting the first input ports 116_1 and 117_1 of the pair of OR gates 116 and 117 to a HIGH state. Therefore, the Boolean logic for an OR gate dictates that no matter what the input signal may be at the second

input ports 116_2 and 117_2 of the first and second OR gates 116 and 117, the respective outputs 116_3 and 117_3 of the OR gates 116 and 117 will always be at a logical HIGH state, i.e., bus traffic noise will be precluded for being coupled to the tuner 140.

The tuner 140 of the receiver 100 comprises a phase-lock loop IC (PLL) 142 having an oscillator (e.g., voltage controlled oscillator (VCO)) 143 coupled to a down converter 144 through a signal path 147. In an instance where a user selects an analog channel, the tuner 140 produces the video and audio IF signals sent to the video and audio processors 122 and 124 for processing of the video and audio information. In an instance where a user selects a digital channel, the tuner 140 produces a digital IF signal (e.g., 5.38 Mhz) that gets forwarded to the digital demodulator 132 to separate out the carrier component of the signal and provide the baseband signal. The baseband signal is then forwarded to the MPEG transport processor 126 where the video and audio substreams are separated for processing at the video and audio processors 122 and 124.

The output of the first OR gate 116_3 is coupled to the input clock line 145 of the phase-lock loop IC 142 in the tuner 140. Furthermore, the output of the second OR gate 117_3 is coupled to the input data line 146 of the phase-lock loop IC 142. Thus, the buffer 114 functions to selectively isolate both phase-lock loop inputs 145 and 146 of the phase-lock loop IC 142 from the IIC bus 118 and the microprocessor 106.

In operation, when the bus expander 108 is sent a command signal from the microprocessor 106 to hold the output control port 109 "HIGH", each OR gate 116 and 117 will logically hold their respective outputs 116_3 and 117_3 HIGH. Thus, the input clock line 145 and the input data line 146 of the phase-lock loop IC 142 are logically in a HIGH state. In an instance where both the serial clock and serial data lines on an IIC bus are held in a HIGH state, no data may be transferred between the two devices. Therefore, in this instance, the traffic noise from the microprocessor 106 that exists when the microprocessor 106 is communicating with other receiver IC's 105 in the system, will be excluded from passing through the input clock and data lines 145 and 146 of the

phase-lock loop IC 142, and will not affect the generation of tones by the VCO 143.

FIG. 2 depicts a flow diagram of a method for isolating the tuner from the bus in accordance with the present invention. The method begins at step 200 and proceeds to step 202, where a user selects a television signal from a control device. At step 204, the television signal is coupled to a down-converter or mixer for further processing.

In step 206, the microprocessor (master) signals the bus expander, via a first IIC command, to set the bus expander output to a LOW state. Henceforth, the phase-lock loop may receive data transmission from the microprocessor, via the SCL and SDA lines. To start data transmission, the microprocessor sets the SDA line of the IIC bus from a steady state HIGH, to a LOW transition, while the SCL is held in a steady state HIGH. Such transition indicates a start condition for the exchange of data bits. The HIGH or LOW state of the data line (SDA) may only change when the clock signal on the SCL line is LOW. At the next clock pulse from the microprocessor, the serial clock line is set LOW, causing the output clock line of the buffer (i.e., first OR gate of FIG.1) coupled to the clock input of the phase-lock loop, to a LOW state.

At each subsequent LOW clock pulse, data may be transmitted over the SDA line, thereby permitting the phase-lock loop IC to receive data transmissions over the IIC bus from the microprocessor. The data transmissions contain information necessary for the phase-lock loop to generate a tone, which facilitates demodulation of a television signal located at a particular channel. As long as the microprocessor sends a repeated START signal, prior to transmitting each byte, the IIC bus remains in a "busy" state. When the microprocessor has completed the data transmission, the microprocessor generates a LOW to HIGH transition on the SDA line, while the SCL is HIGH, to define a stop condition.

In step 208, once the phase-lock loop receives the information necessary to generate the tone, the phase-lock loop locks at a specific frequency designated by the microprocessor. The method proceeds to step 210, where the microprocessor, via a second IIC command from the microprocessor, causes the output on the bus expander to go into a HIGH state. The HIGH state from the

output of the bus expander, thereby causes the buffer to also go into a HIGH state, in a similar manner as described above. At this point, the phase-lock loop is appropriately locked at a specific frequency, and the phase-lock loop is isolated from any further communications (noise) from the microprocessor's activities with other IC's on the IIC bus.

In step 212, the television signal and the locked frequency tone are combined in the down-converter, and an IF signal is produced. Thus, when the tone is mixed with the television signal in the down-converter, a IF signal is produced without any fluctuations in frequency due to microprocessor generated bus noise. In step 214, the IF signal is demodulated (then sent to an MPEG processor to produce video and audio substreams in the instance where the signal is a digital IF signal), and processed to produce the desired audio and video output. At step 216, the method ends, until a user requests a different television channel whereupon the inventive method is repeated.

It should be apparent to those skilled in the art that a novel method and apparatus for excluding noise from an input of a terrestrial television signal tuner has been provided. The buffer device inventively functions to isolate the phase-lock loop IC from noise occurring on the IIC bus. Although various embodiments that incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

CLAIMS

1. An apparatus for isolating a noise intolerant device (140) from a source of noise, comprising:

a processor (106) for producing clock and data signals (SCL, SDA) and a control signal; and

a digital bus (118) that couples said clock and data signals to a buffer (114),

where, in response to said control signal (109), said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device.

2. The apparatus of claim 1, wherein said digital bus is an inter integrated circuit (IIC) bus, and the apparatus further comprises an IIC bus expander (108) for transferring said control signal to said buffer.

3. The apparatus of claim 1, wherein the digital bus comprises

an IIC bus having a clock signal path (SCL) for transferring clock pulses from said processor (106) to said clock inputs of said IIC bus expander (108) and said buffer (114);

a data signal path (SDA) for transferring data from said processor (106) on said data signal path during each of said clock pulses on said clock signal path to said clock and data inputs of said IIC bus expander (108) and said buffer (114); and

wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device (140) from said IIC bus and said processor.

4. The apparatus of claim 3, wherein said noise intolerant device comprises:

a tuner (140), coupled to said clock and data outputs of said buffer device, having a phase-lock (142) loop for generating frequency variable tones, and a down-converter (144) coupled, to said phase-lock loop, for mixing one of a plurality of television signals with a one of said frequency variable tones to produce an IF television signal.

5. The apparatus of claim 4, wherein said buffer (144) comprises:

a first OR gate (116) and a second OR gate (117), each of said first and said second OR gates having a first input (116_1, 117_1) coupled to said output of said IIC bus expander;

a second input (116_2) said first OR gate coupled to a clock signal path of said IIC bus, and a second input (117_2) of said second OR gate coupled to a data signal path of said IIC bus; and

an output (116_3) of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop (142) , and an output (117_3) of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop (142).

6. A television receiver (100) for receiving and processing television signals, apparatus comprising:

a controller assembly (102) comprising an inter-integrated circuit (IIC) bus having a clock signal path (110) and a data signal path (112), a processor (106), coupled to said clock and data paths, an IIC bus expander (109) coupled to said processor via said clock and data paths, and a buffer (114) coupled to an output of said IIC bus expander;

a front-end assembly (130) comprising a tuner (140) having a down converter (144) coupled to a phase-lock loop (142), said phase-lock loop coupled to an output of said buffer (114), at least one demodulator (131, 132) for demodulating said television signals, coupled to said down-converter, such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device; and

at least one video and audio processor (122, 124) for processing said modulated television signals to produce audio and video signals.

7. The apparatus of claim 6, wherein said buffer comprises:

a first OR gate (116) and a second OR gate (117), each of said first and said second OR gates having a first input (116_1, 117_1) coupled to said output of said IIC bus expander;

a second input (116_2) of said first OR gate coupled to said clock signal path of said IIC bus, and a second input (117_2) of said second OR gate coupled to said data signal path of said IIC bus; and

an output (116_3) of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop (143), and an output (117_3) of said second OR gate, being said data output of said buffer (114), coupled to said data input of said phase-lock loop.

8. A method for isolating a phase-lock loop in a tuner of a television receiver, comprising the steps of:

sending (208) a first command from a processor to a phase-lock loop via a digital bus to generate a frequency tone; and

sending (210) a second command to a buffer to isolate said phase-lock loop from said processor, whereby said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device

9. The method of claim 8, wherein said first command sending step further comprises the steps of:

setting an inter-integrated circuit (IIC) bus expander output to a LOW logical state, after receiving a request for a selected television signal from a user, in response to said first command by said processor; and

coupling said phase-lock loop to an IIC bus, for enabling said processor to communicate with said phase-lock loop to generate said frequency tone.

10. The method of claim 9 wherein said coupling step further comprises the step of:

enabling, in response bus expander output, a buffer to couple said phase-lock loop to said IIC bus.

11. The method of claim 9, wherein said second command sending step further comprises the step of:

setting an output of said buffer to a HIGH logical state after said phase-lock loop locks to said single frequency tone, in response to said second command from said processor.

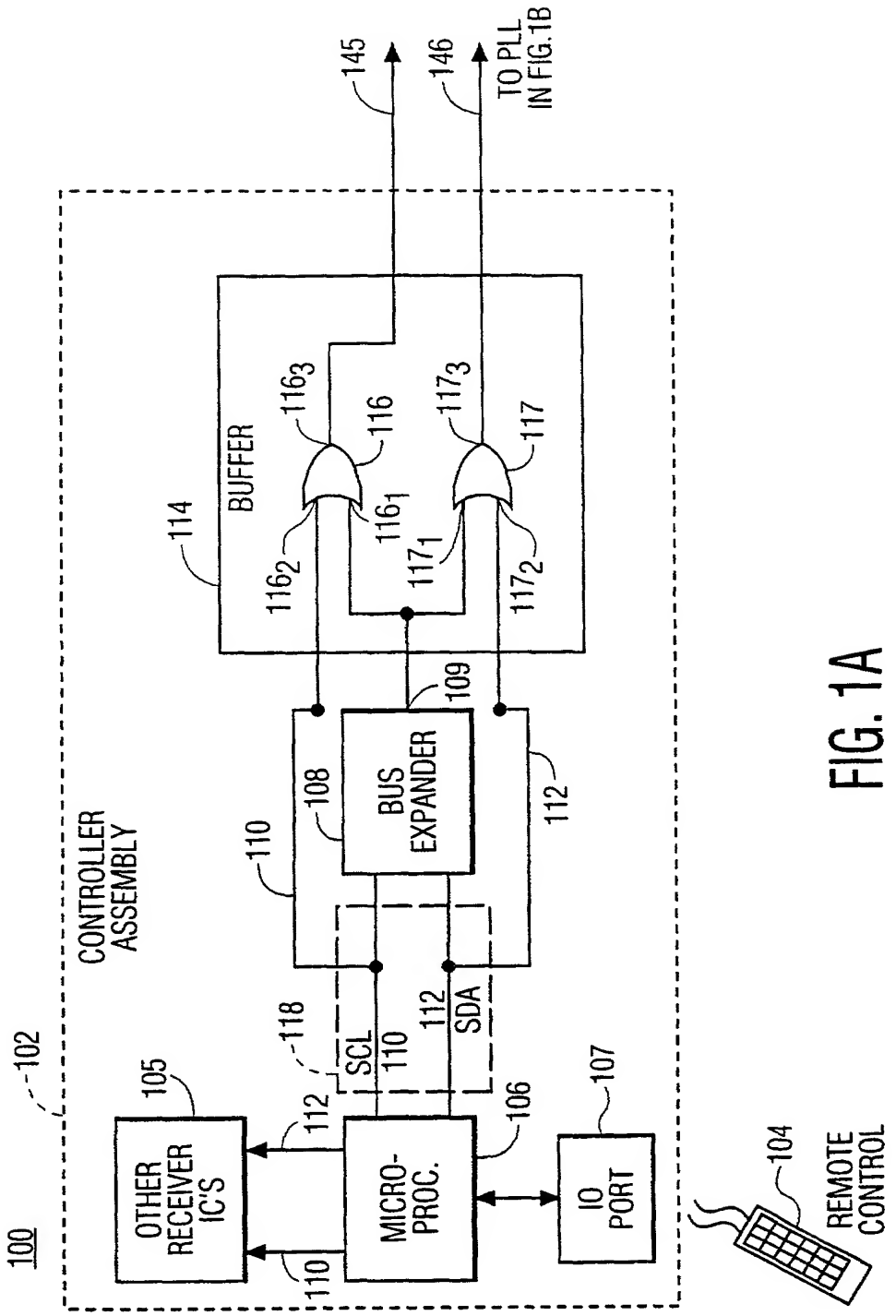
100
102
CONTROLLER ASSEMBLY
OTHER RECEIVER IC'S
105
MICRO-PROC.
106
IO PORT
107
REMOTE CONTROL
104
SCL
SDA
110
112
118
BUS EXPANDER
108
109
BUFFER
114
116
116_1
116_2
116_3
117
117_1
117_2
117_3
145
146
TO PLL IN FIG.1B

FIG. 1A

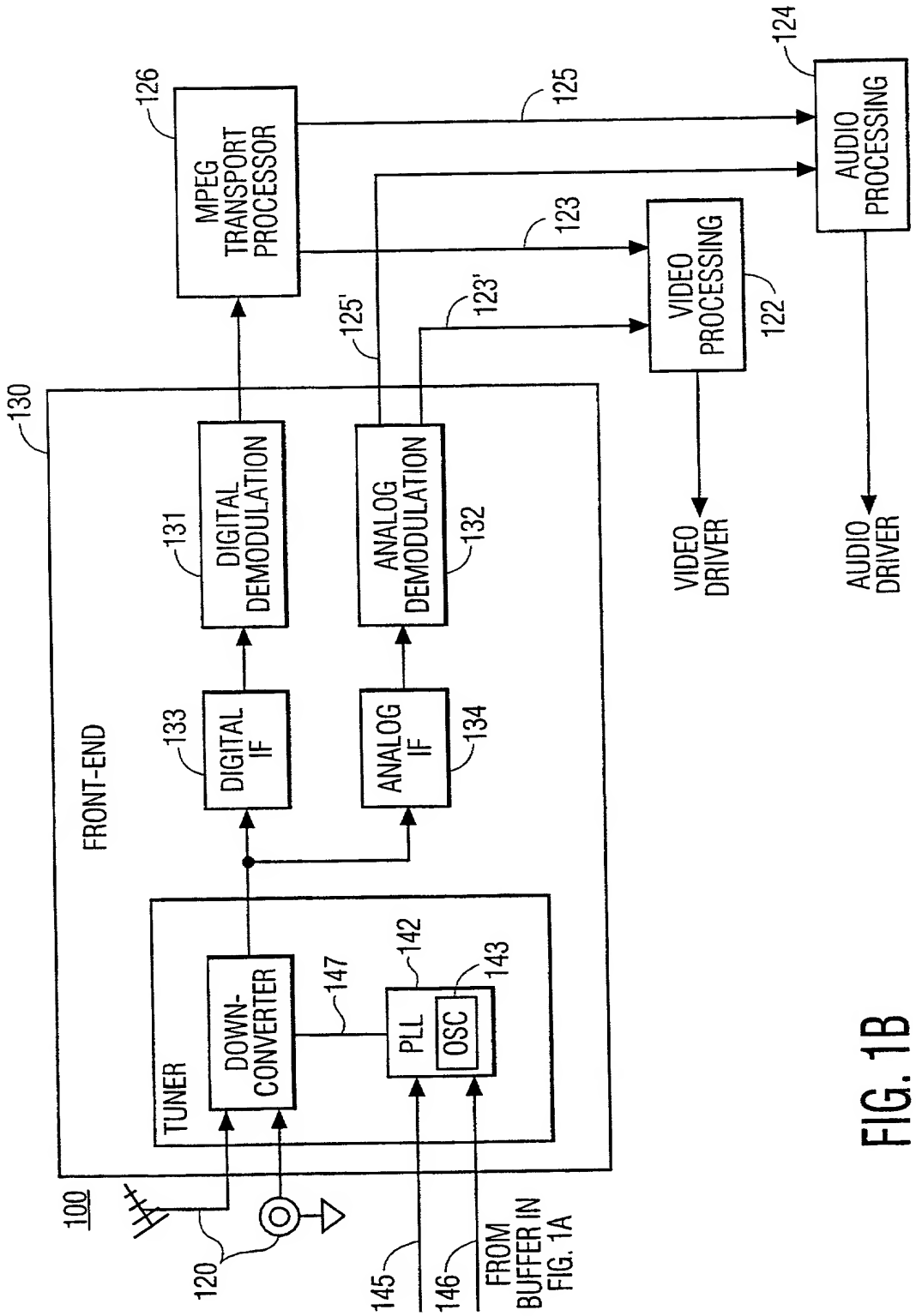
MPEG TRANSPORT PROCESSOR
126
125
AUDIO PROCESSING
124
123
VIDEO PROCESSING
122
123'
125'
130
DIGITAL DEMODULATION
131
ANALOG DEMODULATION
132
VIDEO DRIVER
AUDIO DRIVER
FRONT-END
DIGITAL IF
133
ANALOG IF
134
TUNER
DOWN-CONVERTER
147
PLL
142
OSC
143
100
120
145
146
FROM BUFFER IN FIG. 1A

FIG. 1B

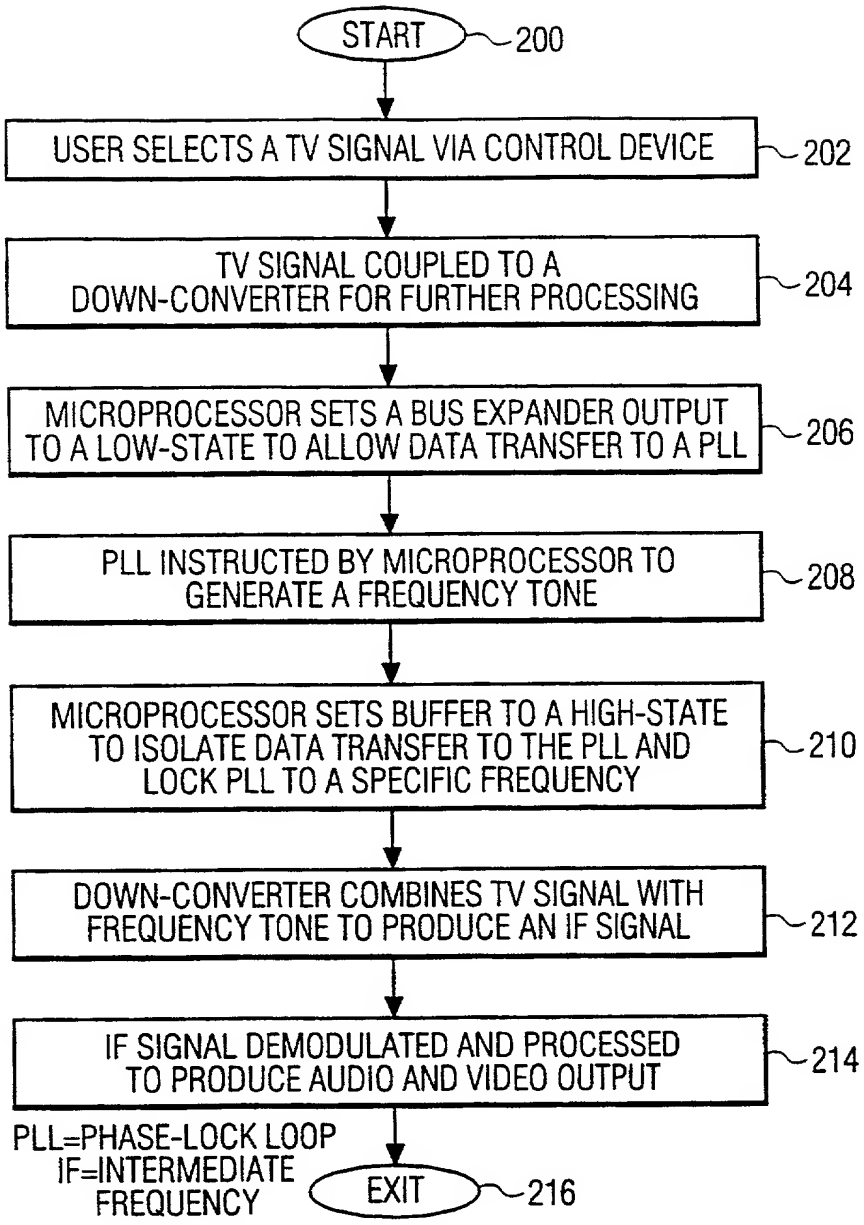
START
200
USER SELECTS A TV SIGNAL VIA CONTROL DEVICE
202
TV SIGNAL COUPLED TO A DOWN-CONVERTER FOR FURTHER PROCESSING
204
MICROPROCESSOR SETS A BUS EXPANDER OUTPUT TO A LOW-STATE TO ALLOW DATA TRANSFER TO A PLL
206
PLL INSTRUCTED BY MICROPROCESSOR TO GENERATE A FREQUENCY TONE
208
MICROPROCESSOR SETS BUFFER TO A HIGH-STATE TO ISOLATE DATA TRANSFER TO THE PLL AND LOCK PLL TO A SPECIFIC FREQUENCY
210
DOWN-CONVERTER COMBINES TV SIGNAL WITH FREQUENCY TONE TO PRODUCE AN IF SIGNAL
212
IF SIGNAL DEMODULATED AND PROCESSED TO PRODUCE AUDIO AND VIDEO OUTPUT
214
PLL=PHASE-LOCK LOOP
IF=INTERMEDIATE FREQUENCY
EXIT
216

FIG. 2

Please type a plus sign (+) inside this box → [+]

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted With Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	RCA 89647
First Named Inventor	David Glen White et al.
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR ISOLATING IIC BUS NOISE FROM A TUNER IN A TELEVISION RECEIVER

the specification of which *(Title of the Invention)*

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) December 22,1999 as United States Application Number or PCT International Application Number PCT/US99/30775 and was amended on (MM/DD/YYYY) July 10, 2001 (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

ApplicationNumber(s)	Filing Date (MM/DD/YYYY)
US 60/143,845	July 15, 1999

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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☐ **Additional inventors are being named on the** _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.